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McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
RIZZUTO, KEVIN P	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 10/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/911,739	YOSHIDA, TOYOHIKO	
	Examiner	Art Unit	
	Kevin P. Rizzuto	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *8 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-18 have been examined.

2. Acknowledgement of papers filed: Amendment on 7/8/2005. The papers filed have been placed on record.

3. The objections to the claims, title and drawings have been overcome via amendments. Therefore, these objections have been withdrawn.

Specification

4. The disclosure is objected to because of the following informalities: reference to incorrect or non-existent item in drawings. Page 10, lines 6-12 refer to MUX 536 outputting a selected data item on signal line, when signal line 104 is not connected to MUX 536. Applicant amended the specification to address one instance of signal line 104 being incorrectly referenced, however, there is another instance of signal line 104 being connected to MUX 536.

Appropriate correction is required.

Maintained Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 7 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Augusteijn et al., U.S. Patent 6,292,883, herein referred to as Augusteijn.

7. As per claim 1, Hammond teaches a data processing device with an instruction translator comprising:

-A processor core: (Figure 1B, PROC 112)

-And a memory interface portion (Figure 1B, preprocessor 130) arranged between said processor core and an external memory (figure1B, IM 120) mapped into a predetermined external memory space.

-Said memory interface portion including a fetch circuit (FTCH 134) for receiving an address value for access to said external memory space from said processor core: (Column 11, lines 9-29 and column 7, lines 18-22)

-And fetching the information at said address in said external memory, said information being an instruction nonnative to said processor an instruction native to said processor or data to be processed: (Column 7, lines 1-44)

-A translator (Converter 132) for translating the instruction nonnative to said processor core fetched by said fetch circuit from said external memory into the native instruction and a select circuit (DET 440) for selectively applying the information read from said external memory space and the instruction prepared by translating the instruction read from said external memory space by said translator to said processor core depending on whether the address value for the access from said processor core to said external memory space is in a predetermined region or not: (Figure 4, column 10, lines 36-56,

column 5, line 64 to column 6, line 8. Specifically, Augusteijn states, "By determining in which region the address of the instruction to be executed lies, the converter can easily detect whether or not conversion is required (native instruction need not be converted) and which conversion means should be used for the conversion." (Col. 6, lines 4-8))

8. Given the similarities between claim 1 and claims 7 and 13, the arguments as stated for the rejection of claim 1 also apply to claims 7 and 13.

Maintained Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 2-4, 8-10 and 14-16 rejected under 35 U.S.C. 103(a) as being unpatentable over Augusteijn et al., U.S. Patent 6,292,883, herein referred to as Augusteijn, in view of IBM Technical Disclosure Bulletin, NN610843, herein referred to as IBM TDB.

11. As per claim 2, Augusteijn teaches the data processing device with the instruction translator according to claim 1, wherein said fetch circuit includes: an address conversion circuit for effecting predetermined conversion on the address for the access from said processor core to said external memory, and a circuit for selectively applying the address sent from said processor core and the address output from said

address conversion circuit to said external memory depending on whether said address is within said predetermined region or not. (The fetch circuit fetches both native (16 or 32-bit) and non-native instructions (8 bit). (Column 8, line 66 to column 9, line 12, column 9, lines 34-36 and column 10, lines 56-67) The fetch/pc counter is described as only incrementing when it is necessary, which depends on which mode the processor is in, non-native or native, it is not necessary to increment and fetch instructions as often when in the non-native mode. (Column 11, lines 41-54) However, no specific address conversion means for fetching is provided, even though the instructions are different sizes, which one of ordinary skill in the art would recognize as a problem when it comes to addressing instructions and data in memory. However, no explicit teaching is given, and thus, Augusteijn leaves the implementation of the fetch circuit up to the designer.

12. IBM TDB discloses that when a processor has a native operating mode with data stored in memory at twice the size of a non-native operating mode, a simple circuit can be added to accommodate the non-native addressing instead of an elaborate program to adjust non-native addressing. The address conversion means are applied selectively depending on which mode the processor is in, native (double precision) or non-native (single precision). The circuit consists of a right shift circuit and selection hardware to determine if the right shift should be made. (Entire IBM TDB and drawing)

13. It would have been obvious to add the address conversion circuit taught by the IBM TDB in order to simply and effectively convert the addresses for the shorter instruction lengths of the non-native code in Augusteijn. This would allow the non-native and native instructions to be addressed in memory without the need for a

complex program to convert all the addressing of the non-native instructions, and therefore there would have been motivation for one of ordinary skill in the art to combine the inventions as described above.

14. Given the similarities between claim 2 and claims 8 and 14, the arguments as stated for the rejection of claim 2 also apply to claims 8 and 14.

15. As per claim 3, Augusteijn, in view of the IBM TDB, teaches the data processing device with the instruction translator according to claim 2, wherein said conversion circuit includes a division circuit for dividing the input address value by n-th (n: natural number) power of 2 and outputting the result. (The right shift performed, as taught by the IBM TDB, is a division by 2, which is a n-th power of 2, and the result is outputted. (See drawings of IBM TDB and documentation)

16. Given the similarities between claim 3 and claims 9 and 15, the arguments as stated for the rejection of claim 3 also apply to claims 9 and 15.

17. As per claim 4, Augusteijn, in view of the IBM TDB, teaches the data processing device with the instruction translator according to claim 3, wherein said division circuit includes a shifter for shifting rightward the input address value by n bits. (The division by 2 that is performed, as taught by the IBM TDB, is carried out by a right-shifter. (See drawings of IBM TDB and documentation)

18. Given the similarities between claim 4 and claims 10 and 16, the arguments as stated for the rejection of claim 4 also apply to claims 10 and 16.

19. Claims 1, 7 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arya, U.S. Patent 5,881,258, in view of Hammond et al., U.S. Patent 5,638,525, herein referred to as Hammond.

20. As per claim 1, Arya teaches a data processing device with an instruction translator comprising:

-A processor core: (Figure 1, processor 102)

-And a memory interface portion (Compatibility Circuit 108, TLB 202 and Branch Condition Check) arranged between said processor core (Processor 102) and an external memory (Memory 110) mapped into a predetermined external memory space: (Figures 1 and 2)

-Said memory interface portion including a fetch circuit for receiving an address value for access to said external memory space from said processor core,(Figure 2, Branch Condition Check receives the PC and Branch Target address)

-And fetching the information at said address in said external memory, said information being an instruction nonnative to said processor an instruction native to said processor or data to be processed: (Column 1, line 60 to column 1, line 16 and Column 3, lines 27-55)

-A translator (Translator 120) for translating the instruction nonnative to said processor core fetched by said fetch circuit from said external memory into the native instruction: (Column 4, lines 51 to column 5, line 43)

21. While Arya teaches that the processor core can process two types instruction sets, an old instruction set that is translated, and a new instruction set that is not

translated, the disclosure only teaches the translation portion of the processor. Therefore, details about the fetching of the old instruction set and the new instruction set are not provided, and thus a select circuit for selectively applying the information read from said external memory space and the instruction prepared by translating the instruction read from said external memory space by said translator to said processor core depending on whether the address value for the access from said processor core to said external memory space is in a predetermined region or not, is not taught by Arya.

22. Hammond teaches a processor that executes multiple types of instruction sets that are stored within different portions of an external memory. Figure 2 shows the two instruction sets in different portions of the memory, the PowerPC 64 bit set starting at address 1000 and the x86 instruction set starting at address 4000. Depending on which section of memory the processor is fetching from, a section of x86 instructions or PowerPC instructions, a selector circuit 540 (figure 5) will choose for the fetched instructions to be translated or not by the Translator 541. The selector circuit selects which instructions are to be sent to the processor core, the translated instructions or the non-translated instructions.

23. It would have been obvious to one of ordinary skill in the art to combine the inventions of Hammond and Arya because the disclosure of Arya is lacking in the description of how the two different instruction sets (old and new) interact with the processor 102, there is only a description of the old instruction set being fetched, translated and processed. Hammond provides means for two instruction sets to reside

in memory, be fetched from memory, translated, and to select between the translated, non-native instructions and the non-translated, native instructions.

24. Given the similarities between claim 1 and claims 7 and 13, the arguments as stated for the rejection of claim 1 also apply to claims 7 and 13.

25. Claims 5, 11 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arya, U.S. Patent 5,881,258, in view of Hammond et al., U.S. Patent 5,638,525, herein referred to as Hammond, further in view of Denman, U.S. Patent 5,784,585.

26. As per claim 5, Arya, in view of Hammond, teaches the data processing device with the instruction translator according to claim 1, however fails to teach wherein a bus width of an instruction bus in said processor core is different from a bus width of a data bus of said external memory; and said select circuit includes: a bus width changing circuit having an input connected to said external memory and an output of the same width as the bus width of the instruction bus of said processor for performing conversion between the bus width of the data bus of said external memory and the bus width of the instruction bus in said processor, and outputting the result, and a multiplexer having inputs connected to the outputs of said bus width changing circuit and said translator, respectively, and an output connected to said instruction bus of said processor core for selectively applying to said processor core an instruction output from said bus width changing circuit and an instruction output from said translator, depending on whether the address value for the access from said processor core to said external memory space is within a predetermined region or not.

27. Denman teaches wherein:

-A bus width of an instruction bus in said processor core is different from a bus width of a data bus of said external memory: (The bus width of memory bus 10 is 16 bits, while the processor core has an instruction bus of 32-bits. (Figure 1, column 2, lines 47-56 and column 3, lines 7-22))

and a select circuit (MUX 13) includes:

-A bus width changing circuit (latches 11-1 to 11-4 and their controlling circuitry) having an input connected to said external memory and an output of the same width as the bus width of the instruction bus of said processor for performing conversion between the bus width of the data bus of said external memory and the bus width of the instruction bus in said processor: (Figure 1, column 2, line 47 to column 3, line 22, and column 1, lines 34-50))

-And outputting the result, and a multiplexer having inputs connected to the outputs of said bus width changing circuit (Latches 11-1 to 11-4's output bus 12A) and a translator (compressed instruction decoder 18 without output bus 19), respectively, and an output (bus 15) connected to said instruction bus of said processor core (ARM Core 14) for selectively applying to said processor core an instruction output from said bus width changing circuit and an instruction output from said translator: (Figure 1, column 2, line 47 to column 3, line 22, and column 1, lines 34-50))

-Depending on whether the instruction needs translation or not (Column 4, lines 7-31).

28. It would have been obvious to one of ordinary skill in the art to add the bus-width changing circuit (Latches 11-1 to 11-4) because the reduction in bus width between the

memory interface and memory, and memory width. This reduction in width reduces space needed on the chip for bus routing and provides a cost reduction as well. (Column 1, lines 34-50)). It also would have been obvious to add the multiplexer 13 of Denman to select between the instructions output from the translator 120 and the instructions output from the bus width changing circuit because the processor of Arya, in view of Hammond, only needs one of the two at a time. Hammond already teaches the Demultilplexer to select where the fetched data from memory is sent to, it would have been obvious to one of ordinary skill in the art to add a multiplexer 13 to select one of the two instruction buses to send on to the processor core as is taught in Denman, since only one instruction bus has valid data and is needed.

29. Given the similarities between claim 5 and claims 11 and 17, the arguments as stated for the rejection of claim 5 also apply to claims 11 and 17.

30. Claims 6, 12 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arya, U.S. Patent 5,881,258, in view of Hammond et al., U.S. Patent 5,638,525, herein referred to as Hammond, further in view of Jouppi, U.S. Patent 5,386,547.

31. As per claim 6, Arya, in view of Hammond, teaches the data processing device with the instruction translator according to claim 1, wherein said processor core has an instruction bus, an instruction address bus, a data bus and a data address bus: (Arya explicitly teaches an instruction data bus and instruction address bus, shown in figure 2. However, in figure 1 of Arya, the Data Cache 106 is depicted with only one unlabeled bus connected to the processor portion and one bus connected to the memory. It is inherent that the bus connecting the Data cache 106 to memory 110 contains both an

address bus and data bus, or else the system would not function properly, i.e., it would either supply an address and not be able to receive data, or receive data and not be able to specify an address.

32. However, Arya, in view of Hammond, is silent on the construction of the memory device, and it is not clear whether it is capable of multiple/simultaneous reads/writes or if it is only capable of a single read/write at a time, i.e., whether or not the Instruction Cache and Data Cache can access the memory simultaneously or not. Therefore, there is no hardware taught to select between the two inputs to the memory (Data address bus and Instruction address bus), and therefore Arya, in view of Hammond, fails to teach said data processing device further including:

-A multiplexer having inputs connected to said instruction address bus and said data address bus, respectively,

-For selecting said instruction address bus or said data address bus for application to said fetch circuit in response to the control signal applied from said processor core,

-And a second multiplexer for electrically coupling said memory bus to said instruction bus or said data bus, in response to said control signal applied from said processor core.

33. However, Jouppi teaches a memory system very similar to Arya, in view of Hammond. In figure 3 of Jouppi, a separate data and instruction cache is shown, each with an address bus output to a higher level of memory that consists of a mix of instructions and data, just as taught in Arya. Jouppi teaches the specifics of the system,

including a multiplexer 132 to select between the two addresses input to the higher level combined instruction/data memory, which allows a particular address to be chosen to access the higher memory.

34. It would have been obvious to add the multiplexer 132 as taught in figure 3 of Jouppi and column 5, lines 1-53, to allow bus arbitration between the data and instruction cache and the memory, of Arya, in view of Hammond. Since Arya, in view of Hammond, is silent on the interface between the instruction and data addresses from the caches to the memory 110, it would have been obvious to add the multiplexer 132 of Jouppi because a multiplexer is a simple, cheap, and well known solution to two buses being input to one piece of hardware.

35. Given the similarities between claim 6 and claims 12 and 18, the arguments as stated for the rejection of claim 6 also apply to claims 12 and 18.

Response to Arguments

36. Applicants arguments filed on 7/8/2005 have been fully considered but they are not found persuasive.

37. Applicant argues the novelty/rejection of claims 1, 7 and 13.

> "The reference [Augusteijn] does not disclose 'selectively applying the data read from said external memory space and the instruction prepared by the translation of the instruction read from said external memory space to said processor core depending on whether the address value for the access from said processor core to said external memory space is in a predetermined region or not,' recited in claims 1, 7 and 13 (emphasis added)."
>
> "Examiner's cited portions in Augusteijn et al. merely describes selecting native instructions or instructions converted from non-native instructions (see column 10, lines

36-56; and column 5, line 64 to column 6, line 8 of Augusteijn et al.). Therefore, it is apparent that Augusteijn does not disclose, and the Examiner did not point out where the reference disclose, conditions to select the native instructions or the converted instructions, as recited in the claims, i.e., 'depending on whether the address value for the access from said processor core to said external memory space is in a predetermined region or not.'"

38. These arguments are not found persuasive for the following reasons:

a. To clarify, applicant's attention is directed towards the previously cited portions of Augusteijn et al., that is, column 10, lines 36-56; and column 5, line 64 to column 6, line 8, where it is stated:

> "***By determining in which region the address of the instruction to be executed lies, the converter can easily detect whether or not conversion is required (native instruction need not be converted) and which conversion means should be used for the conversion***." (Col. 6, lines 4-8))
>
> "The address range of the instruction memory 120 is divided into several sub-ranges. ***An address sub-range is reserved for storing virtual machine instructions of only one virtual machine***. Preferably, an ***address sub-range is also reserved for storing native instructions...***In this embodiment the ***selection data indicates for each of the defined address sub-ranges which one of the conversion means 400, 410 or 420 should be used*** for converting an instruction fetched by the instruction fetcher to native instructions....If also ***native instructions are stored in the instruction memory 120, the detector 440 ensures that these instructions are directly supplied to the feeder 136*** for supply to the microcontroller core 114."

b. Thus Augusteijn et al. clearly anticipates the specified limitation Applicant is presently arguing and Examiner clearly pointed out where the reference disclosed the limitations taught by Augusteijn. Furthermore, it was specified that

the "DET 440" of figure 4 that Augusteijn taught was the claimed "select circuit".

(See original Non-Final Office Action, page 5, line 1.)

39. Applicant argues the novelty/rejection of claims 1, 7 and 13.

"Although the Examiner asserted that selector circuit (demultiplexer) 540 of Hammond et al. corresponds to the above limitation, Applicant does not respectfully disagree with the Examiner. The following is reproduction of column 14, line 67 to column 15, line 6 of Hammond et al."

> "The selection of demultiplexer 540 is based on the signal received by demultiplexer 540 from decoder 543. The first signal from decoder 543 causes demultiplexer 540 to select translator 541 and the first instruction set mode. A second signal from decoder 543 causes demultiplexer 540 to select translator 541 and the first instruction set mode. A second signal from decoder 543 causes demultiplexer 540 to select instruction cache 542 and the second instruction set mode (emphasis added)."

"It is apparent that Hammond et al. does not teach causing demultiplexer 540 to select translator 541 or instruction cache 520 depending on whether the address value for the access from said processor core to said external memory space is in a predetermined region or not. Hammond et al. merely describes selecting translator 541 and the first instruction set mode when the first signal from decoder 543 is received, and selecting the instruction cache 542 and the second instruction mode when the second signal is received. This description does not suggest the condition 'whether the address value for the access from said processor core to said external memory space is in a predetermined region or not,' recited in claims 1, 7 and 13."

40. These arguments are not found persuasive for the following reasons:

c. To clarify, applicant's attention is directed towards col. 15, lines 41-52. The decoder does provide the signal that causes the demultiplexer 540 to either select the translator or not. However, the decoder causes this signal to be sent when a jmpx instruction or x86jmp instruction is decoded. These two instructions have associated predetermined target addresses, and depending on where they are jumping, either x86 code or non-x86 code, the selector receives the appropriate signal to select the translator or to not select the translator.

d. Furthermore, the x86 code and non-x86 code are in predetermined regions as shown in fig. 2 and col. 6, lines 40-58 and col. 8, lines 53 to col. 9, line 15. The jmpx and x86jmp instructions have an associated target address that is determined before the change in instruction fetching can take place. Depending on which section of memory the processor is fetching from, a different type of instruction is being fetched (native or non-native), the selector, dependent on which type of code is being fetched, will either select for translation or not. Therefore, dependent on which section of memory (predetermined regions) the processor is fetching from, the demultiplexer is either selecting to send instructions to the translator or the instruction cache.

Conclusion

2. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin P Rizzuto whose telephone number is (571) 272-4174. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

KPR

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100